CLAIMS

1. An electrical contact of an optoelectronic semiconductor chip (1), comprising:

a mirror layer (2), comprised of a metal or a metal alloy adapted to be formed over the semiconductor chip;

a protective layer (3) over said mirror layer (2);

a layer sequence of a barrier layer (4) and a coupling layer (5) over said protective layer and a solder layer (8).

2. The electrical contact as claimed in claim 1, which includes a wetting layer (6) between the coupling layer (5) and the solder layer (8).

3. The electrical contact as claimed in claim 1, which is applied to a surface of a semiconductor chip (1) having a nitride compound semiconductor material.

4. The electrical contact as claimed in claim 1, in which the mirror layer (2) contains silver, aluminum or platinum.

5. The electrical contact as claimed in claim 1, in which the mirror layer (2) is between 70 nm and 130 nm thick.

6. The electrical contact as claimed in claim 1, in which a layer (13) of an electrically conductive material between 0.1 and 0.5 nm thin is included between the

semiconductor chip (1) and the mirror layer (2) to improve the adhesion of the mirror layer (2).

7. The electrical contact as claimed in claim 6, in which the surface of the semiconductor chip (1) has a nitride compound semiconductor material, the mirror layer (2) contains Al or Ag, and the thin layer (13) contains Pt, Pd or Ni.

8. The electrical contact as claimed in claim 1, in which the protective layer (3) contains titanium or platinum.

9. The electrical contact as claimed in claim 1, in which the protective layer (3) is between 5 nm and 15 nm thick.

10. The electrical contact as claimed in claim 1, in which the barrier layer (4) completely covers the mirror layer (2) and the protective layer (3).

11. The electrical contact as claimed in claim 1, in which the barrier layer (4) contains TiW(N).

12. The electrical contact as claimed in claim 1, in which the barrier layer (4) is between 300 nm and 500 nm thick.

13. The electrical contact as claimed in claim 1, in which the coupling layer (5) contains titanium.

14. The electrical contact as claimed in claim 1, in which the coupling layer (5) is between 30 nm and 70 nm thick.

15. The electrical contact as claimed in claim 2, in which the wetting layer (6) contains platinum.

16. The electrical contact as claimed in claim 2, in which the wetting layer (6) is between 70 nm and 130 nm thick.

17. The electrical contact as claimed in claim 2, in which a gold layer (7) is applied to the wetting layer (6).

18. The electrical contact as claimed in claim 1, in which a gold layer (9) is applied to the solder layer (8).

19. The electrical contact as claimed in claim 18, in which the gold layer (9) applied to the solder layer (8) is approximately 30 nm to 70 nm thick.

20. The electrical contact as claimed in claim 1, which is adapted for connection of the semiconductor chip (1) to a carrier body, the material of the solder layer (8) being suitable for forming an alloy with the material of the carrier body.

21. The electrical contact as claimed in claim 20, in which the solder layer (8) contains AuGe and the carrier body contains Ge.

22. The electrical contact as claimed in claim 20, in which the solder layer (8) contains AuSi and the carrier body contains Si.

23. The electrical contact as claimed in claim 6 which is adapted for connection of the semiconductor chip (1) to a carrier body, the material of the solder layer (8) being suitable for forming an alloy with the material of the carrier body, and wherein said thin layer (13) comprises palladium or a nickel oxide.

24. A method for producing an electrical contact of an optoelectronic semiconductor chip (1), comprising:

providing a mirror layer (2), comprised of a metal or metal alloy, over the semiconductor chip;

providing a protective layer (3) over said mirror layer;

providing a layer sequence of a barrier layer and a coupling layer (5) over said protective layer; and

providing a solder layer (8) over said layer sequence.

25. A method for producing an electrical contact as claimed in claim 24, in which the contact is patterned by means of a lift-off technique.

26. The method as claimed in claim 25, in which a mask layer (10) applied to the semiconductor chip (1) for the lift-off technique is provided with an undercut, the mirror layer (2) is vapor-deposited in a directed manner and the barrier layer (4) is

applied by an undirected, covering coating method in such a way that the barrier layer (4) completely covers the layers lying under it.

27. A method for producing an electrical contact as claimed in claim 24, wherein a layer (13) of an electrically conductive material between 0.1 and 0.5 nm thin is applied to the semiconductor chip (1) before the application of the mirror layer (2) to improve the adhesion of the mirror layer (2).

28. The method as claimed in claim 27, wherein the surface of the semiconductor chip (1) has a nitride compound semiconductor material, the mirror layer (2) contains Al or Ag, and the thin layer (13) contains Pt, Pd or Ni.

29. The method as claimed in claim 24, wherein said mirror layer is comprised of silver, and the method further comprising annealing at approximately 300°C to improve adhesion of said mirror layer to the semiconductor chip.

30. The method as claim in claim 24, wherein providing said layer sequence comprises providing said barrier layer over said protective layer, and providing said coupling layer over said barrier layer.

31. The electrical contact as claimed in claim 1, wherein said layer sequence comprises said barrier layer over said protective layer, and said coupling layer over said barrier layer.

32. The electrical contact as claimed in claim 20, wherein said alloy is a eutectic alloy.